IN THE CLAIMS:

Please amend each of independent claims 1, 3 and 4 as follows to more clearly distinguish over the applied prior art, and amend claim 2 as follows to correct an antecedent basis error therein.

1. (currently amended) A data processing system allowing a master processor to access a memory by using a slave processor to access the memory while the master processor continues other processing tasks while the slave memory accesses the memory and writes the data from memory to the master processor comprising: a master processor; a slave processor; a memory; and a bus subsystem interconnecting the master processor, the slave processor, and the memory; wherein the master processor is configured to generate, in response to a memory access instruction, a read request comprising a read command for execution by the slave processor to read data stored in a location in the memory specified by the memory access instruction while the master processor continues other processing tasks while the slave processor accesses the memory and writes the data from memory to the master processor, and to write the read request to the slave processor via the bus subsystem, and the slave processor is configured to execute the read command received in the read request from the master processor to obtain the data stored at the specified location in the memory and to write the data obtained to the master processor via the bus subsystem while the master processor continues other processing tasks.

2. (currently amended) A data processing system as claimed in claim 1, wherein the bus subsystem ~~system~~ comprises two buses interconnected by a bridge device and the slave processor is integrated in the bridge device.

3. (currently amended) A disk controller comprising: a master processor; a slave processor; a memory; and a bus subsystem interconnecting the master processor, the slave processor, and the memory; wherein the master processor is configured to generate, in response to a memory access instruction, a read request comprising a read command for execution by the slave processor to read data stored in a location in the memory specified by the memory access instruction while the master processor continues other processing tasks while the slave processor accesses the memory and writes the data from memory to the master processor, and to write the read request

to the slave processor via the bus subsystem, and the slave processor is configured to execute the read command received in the read request from the master processor to obtain the data stored at the specified location in the memory and to write the data obtained to the master processor via the bus subsystem while the master processor continues other processing tasks.

4. (currently amended) A method for reading data from a memory in a data processing system comprising a master processor, a slave processor, a memory, and a bus subsystem interconnecting the master processor, the slave processor, and the memory, the data processing system allowing a master processor to access a memory by using a slave processor to access the memory while the master processor continues other processing tasks while the slave memory accesses the memory and writes the data from memory to the master processor; the method comprising:

generating, by the master processor, in response to a memory access instruction, a read request comprising a read command for execution by the slave processor to read data stored in a location in the memory specified by the memory access instruction while the master processor continues other processing tasks while the slave processor accesses the memory and writes the data from memory to the master processor;

writing, by the master processor, the read request to the slave processor via the bus subsystem;

executing, by the slave processor, the read command received in the read request from the master processor to obtain the data stored at the specified location in the memory while the master processor continues other processing tasks; and,

writing the data obtained to the master processor via the bus subsystem.